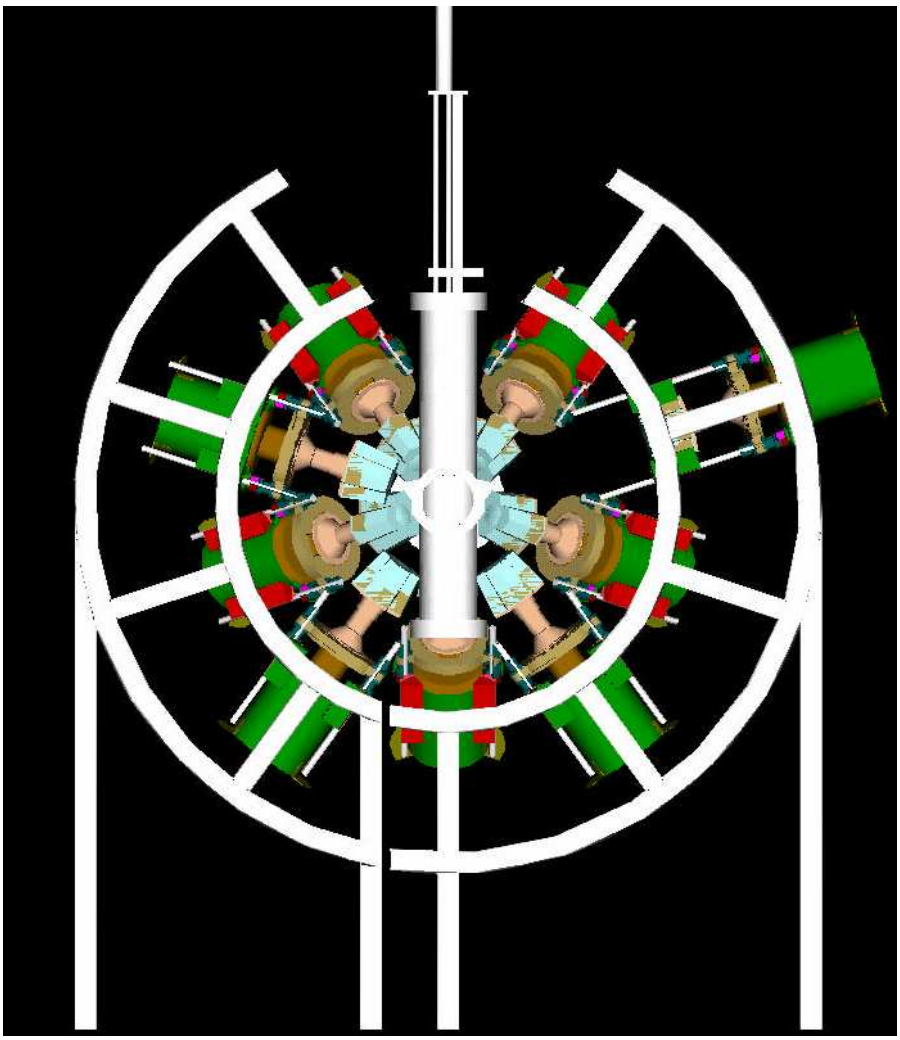
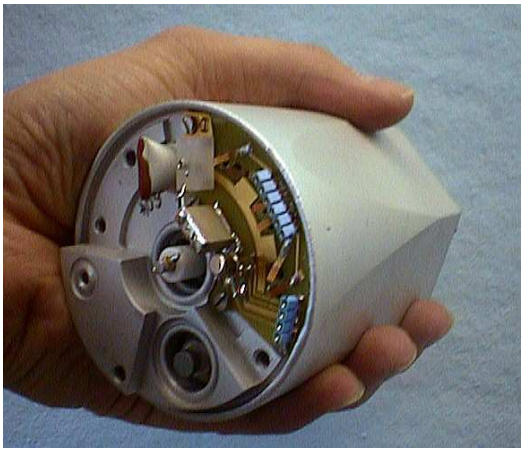
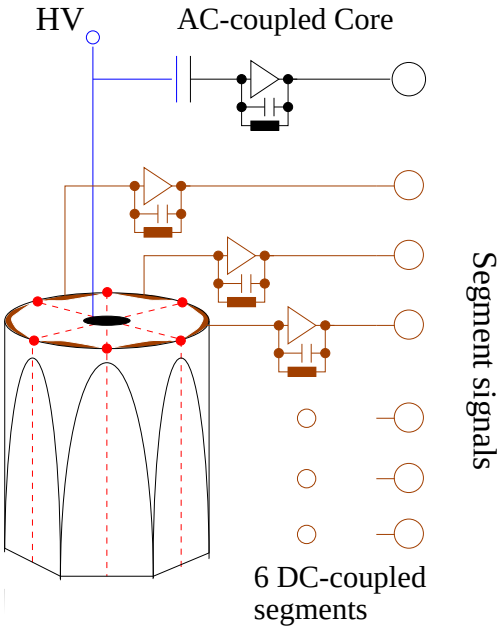
Miniball at RISING



- **Current status:**
  → **24** Ge crystals, **six**-fold segmentation
  housed in **8** cryostats (all triples).
- **Future:**
  → **28** Ge crystals, **six**-fold segmentation
  3 Ge crystals, **twelve**-fold segmentation
  housed in **10** cryostats (9 triple, 1 quad).

The Miniball Capsule



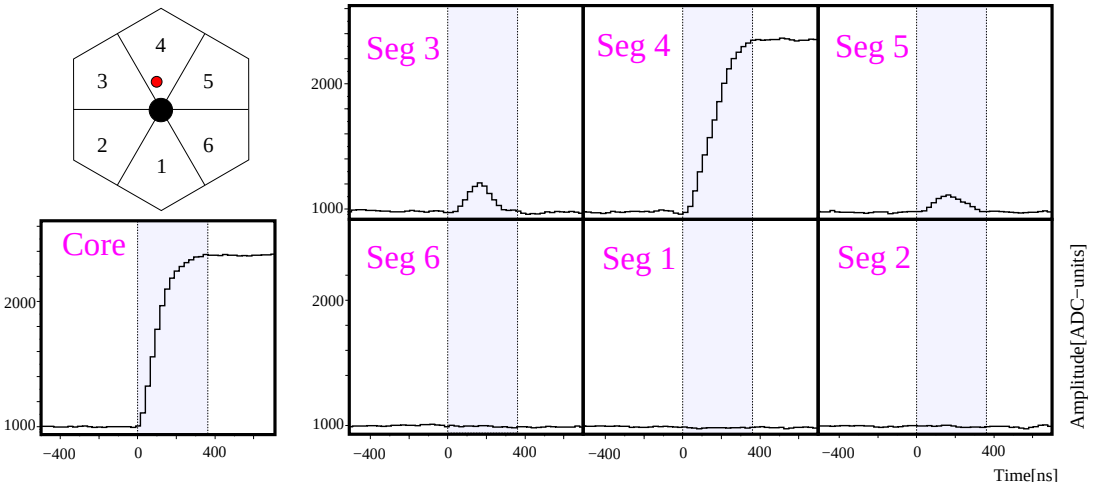


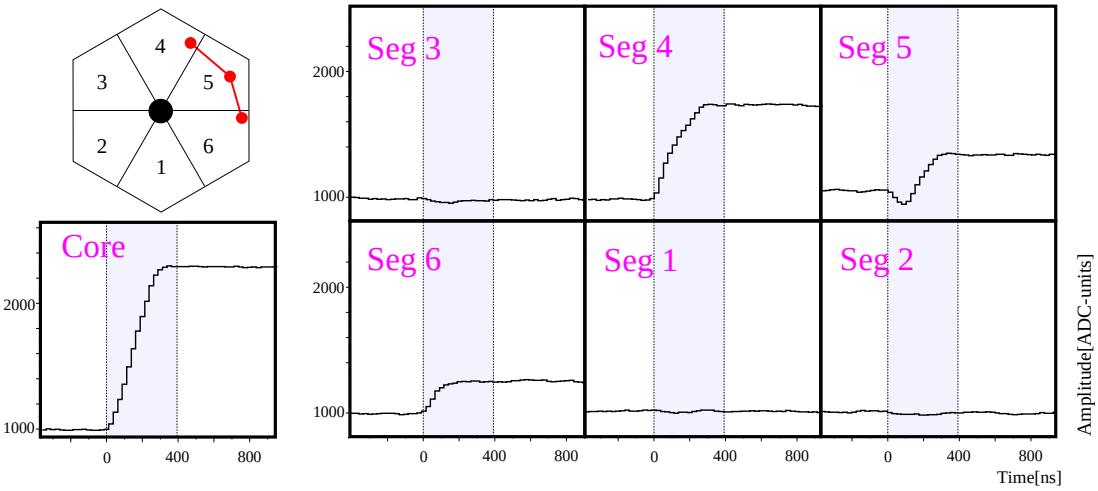
- **6-fold segmented Ge crystal.**
  → **SEVEN signals - core + 6 segments.**

- **12-fold segmented Ge crystal.**
  → **Extra segmentation is in the depth.**
  → **THIRTEEN signals - core + 12 segments.**

- **Only one output per channel.**
  → **No separate energy and time signals.**

Signals And PSA



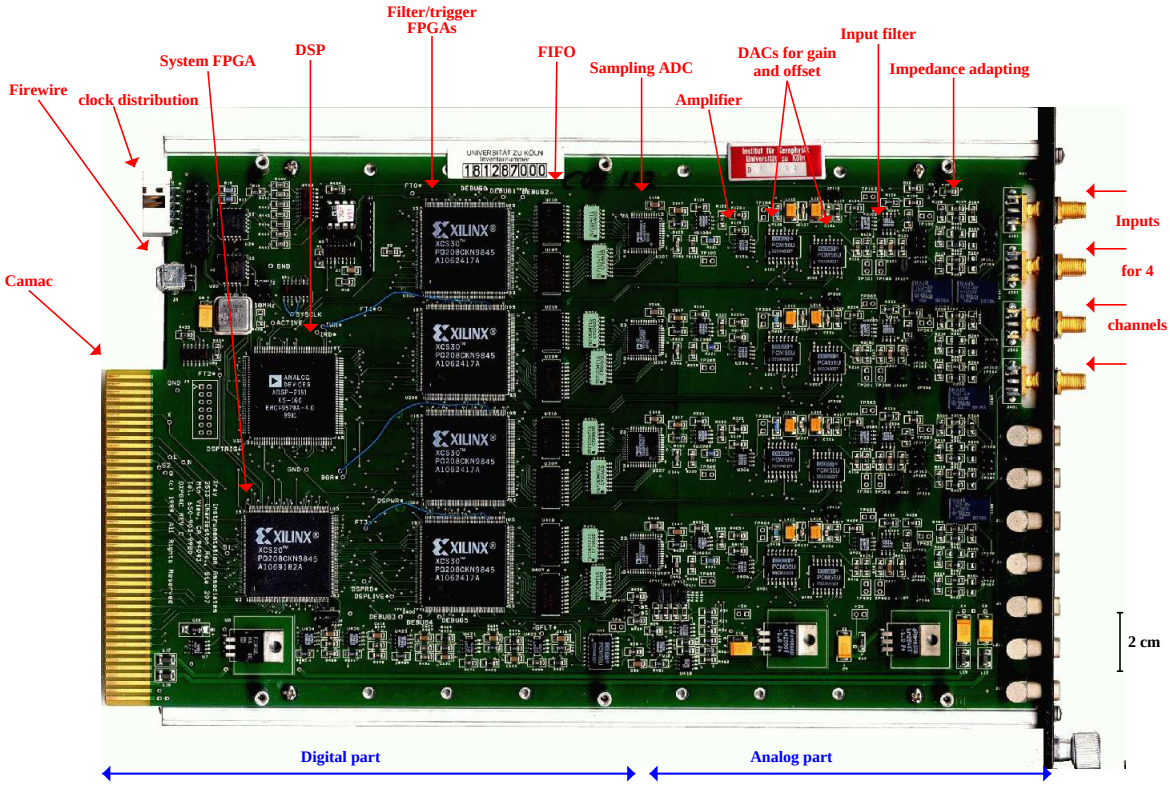


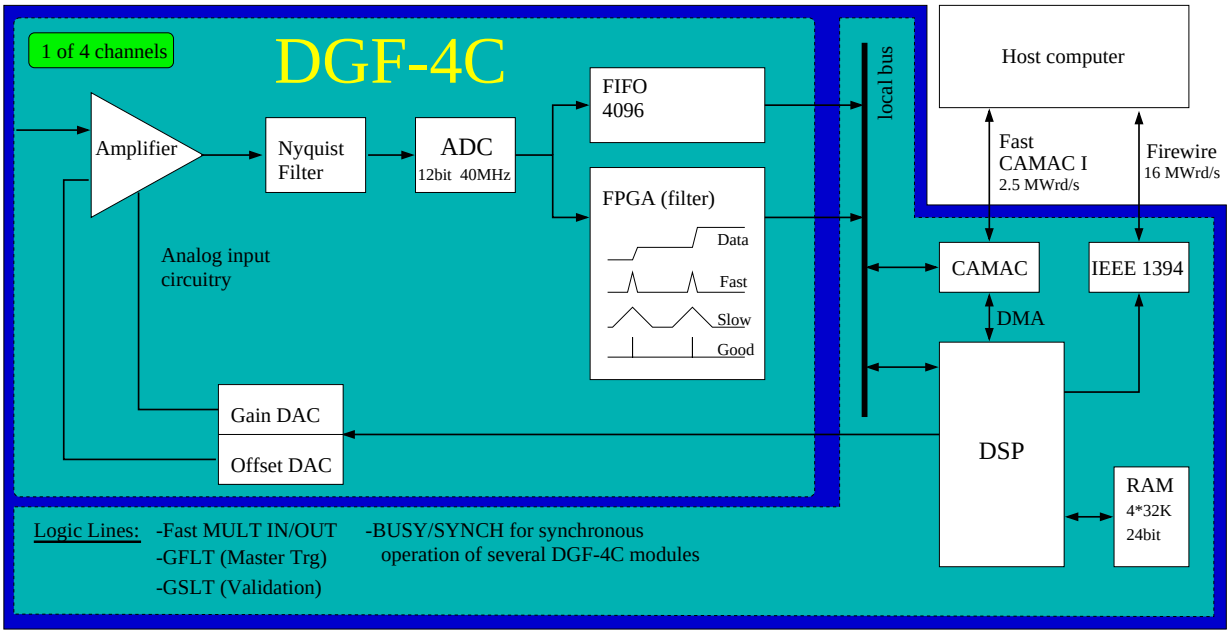
- **Mirror charges in segments give position information.**
- **They can be positive, negative or negligible.**
- **The absence of a mirror charge is also important information.**

→ Only the core provides a reliable trigger.

→ Trigger on core. Always read segments.

The Digital Gamma Finder



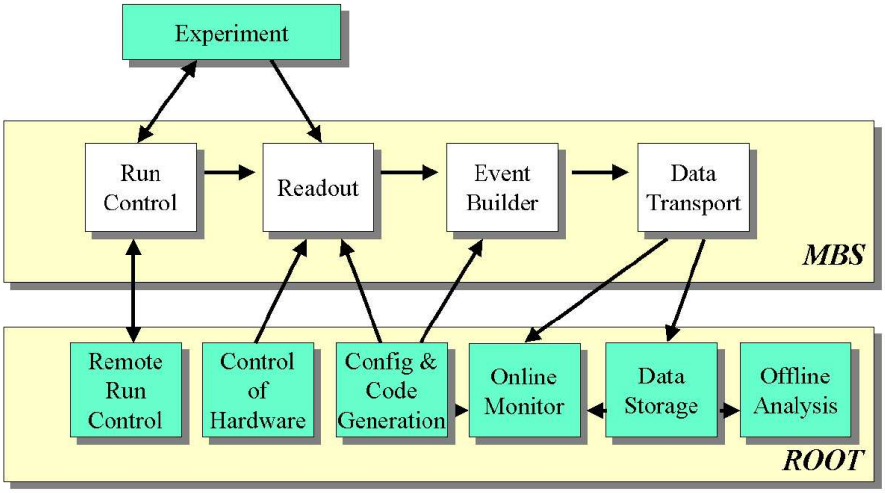


http://www.xia.com

Digital Gamma Finder

- 4 channels per module.
  → Need 2 modules per capsule (4 for 12-fold segmented).
- Raw preamp signal as input.
- Amplifier to adjust gain and offset to match signal to ADC range.
- 40 MHz sampling ADC.
- Separate fast (timing) and slow (energy) filters implemented digitally in FPGA.
- FPGA is real time (essentially dead-time free).
- Validation after signal (about 9 microseconds after).
- DSP processes validated events. Only these events contribute to dead time.
- DSP performs post processing, pulse-shape analysis (Martin Lauer's code), buffering etc.
- Readout via camac through CC32/VC32 controller from VME.
- Get 8 kword buffer: energy, time, PSA parameters (39 words per event if all 4 channels fire).

The Marabou software (The MBS interface)



- **Miniball uses Marabou data acquisition (Rudi Lutter, TU Munich).**
  → Uses MBS for readout.
  → Uses root for analysis.
- **CES RIO2-8062 Power PC running LynxOS in VME crate.**
  → VC32/CC32 interface to CAMAC crate (one per crate).
  → GSI trigger module.
- **Developed in collaboration with GSI (Nik Kurz).**

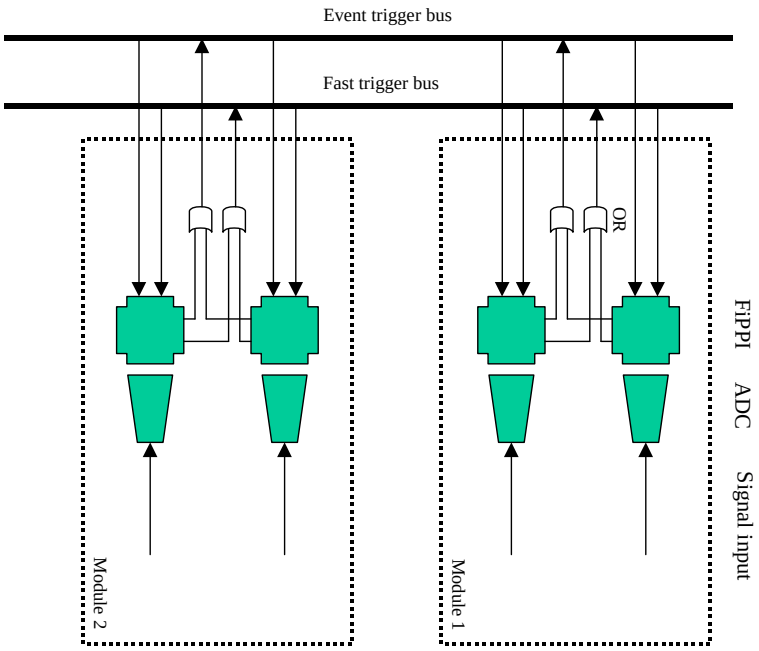
Timestamping in Miniball

- **DGF-4C uses a 40 MHz clock.**
  - → **For Miniball, 40 MHz generated externally (Needed due to error on DGF-4C Rev. D board).**
- **DGF-4C has 48 bit counter (enough for 81 days).**
  - → **But, part counted by FPGA, part by DSP, so full 48-bit must be reconstructed by software.**
- **External 40 MHz Clock (George Pascovici, Cologne).**
  - → **Master clock in one crate, slaves in the others (Or we could make all of them slaves).**
  - → **50 ppm accuracy of quartz oscillator at the moment and could be improved to 10 ppm.**
  - → **Distributed to DGF-4C Rev. D modules by flat cables (3 per crate, up to 8 modules per cable).**
  - → **DGF-4C Rev. E is different. Error on board supposedly corrected - not tested.**
- **Modules synchronised by BUSY-SYNCH loop**
  - → **Each module gives BUSY output when not acquiring. Logical OR of BUSYs fanned out to SYNCH inputs. DGF can be told to zero counter on SYNCH.**

Matching Miniball and RISING timestamps

- **Different timestamp clock frequencies.**
  - → **Miniball works at 40 MHz determined by DGF.**
  - → **RISING at 50 MHz determined by Titris module.**
- **RISING uses Titris module.**
  - → **No clock input or output to/from Titris.**
  - → **So cannot use common clock.**
- **Miniball clock is 50 ppm**
  - → **Could improve to 10 ppm with better oscillator.**
  - → **Probably not good enough on its own.**
- **Plan is to zero both at start of each spill.**
  - → **We will acquire a reference signal in both and compare the timestamps.**
  - → **Similar to timestamping of analogue electronics at CERN.**
- **Problem needs some work still.**

Trigger distribution



- **Core must trigger segments.**
  → **Six-fold segmented capsule needs 2 DGFs (twelve-fold segmented capsule needs 4 DGFs) with all channels triggered by core.**

- **DGF-4C has a trigger/clock bus at rear of module.**
  → **Need to connect clock between all modules but trigger only between modules for same capsule.**

- **Rev. D and Rev. E are different.**
  → **For Rev. D use flat cable with wires 7-10 cut between capsules but present between modules for same capsule.**
  → **For Rev. E use separate wires for clock and trigger in a daisy chain.**

Trigger/gate Logic

- **DGF provides fast Mult Out signal.**
  - → **+35 mVolt per channel hit.**
  - → **Using Mult In, we can create analogue sum.**
  - → **This signal comes from leading edge trigger.**
  - → **Warning - there is a lot of jitter on this signal.**

- **External logic can make a decision based on this signal.**
  - → **Most events where two capsules in a cluster were hit are scattering events.**
  - → **In Cologne we cascade Mult Out signals for each core in a single cluster.**
    So we have one signal per cluster.
  - → **At CERN we gate the Ge detectors with the beam gate or with particle-gamma coincidence.**
    Rising would be similar.

- **Gate (GFLT) is applied after slow filter.**
  - → **i.e. about 9 microseconds after fast trigger.**
  - → **It is a NIM signal.**

DGF-4C Rev. D vs. Rev. E

- Major difference due to error on Rev. D board.
  → (the clock bus was incorrectly terminated)
- This error corrected on Rev. E board.
- The way we use the Rev. D modules is a workaround.
  → This will not work on Rev. E.
  → We have tested Rev. D and Rev. E separately
  but not together.
- Differential non-linearity much better in Rev. E.
- Rev. E has 14 bit ADC, Rev. D only has 12 bit.
- Acquisition software should be identical for both revisions.
- But Xia code is different.
  → So user DSP code for PSA (Martin Lauer) may need to be updated.